Semiconductor Processes II

Module Title:	PH5092 – Semiconductor Processes II
Module Status[1]**:**	Available in second semester 2011/2012 academic year (Spring 2012)

Generic Module Information

Name of module owner/lecturer?	Dr. Arousian Arshak & Prof. Khalil Arshak
Delivery mode: e.g. on-site, on-line, mixed-mode, intensive block delivery. For on-site specify contact hours per week	**For Limerick located students:** on-site in UL: 2 hours lectures per week, and 1 hour of tutorial per week. **For students from other locations:** Intensive block delivery mode, in UL plus course materials available online via ICGEE VLE.
Duration of the module:	1 semester
Assessment methods and weightings where relevant:	20% project 80% written exam
Pass standard:	30%
Penalties for late submission of continuous assessment work:	none
Number of ECTs or institutional credits assigned to the module:	6 ECTs
Course Content or Syllabus	***Rational*** • The purpose of the module is to introduce advanced CMOS process technology and the problems associated with the device fabrication as the technology moves towards 30 nm features and below ***Syllabus*** • CMOS process flow: CMOS fabrication steps, active region formation, shallow trench isolation, n and p well formation. Gate formation: threshold voltage, control of Vth in n and p channel MOS devices, tip or LDD formation (hot electrons), sidewall spacer. • Source and drain formation: contact and interconnect formation, multilevel metal formation for ULSI, RC time delay. Surface contaminants: particles, metallic contaminants, organic contaminants, native/chemical oxide, and moisture. • Cleaning processes: surface characteristics, wet cleaning, dry cleaning, supercritical fluid cleaning, and lamp cleaning-surface refreshing. Cleaning /Etching Chemistries]: contamination reduction, gettering (intrinsic and extrinsic). • Chemical Mechanical Polishing (CMP): SiO2 inter-level

[1] Is the module available, what is the planned start date?

	dielectric layers planarization, tungsten plug formation and shallow trench isolation. Dual Damascene: trench first approach, via first approach, optical proximity correction. • High and low K dielectrics: silicon on insulator, ultra thin oxides, gate dielectrics, degradation mechanisms, nitroxides, fluorinated oxides, shallow junction formation, transient enhanced diffusion. • Electrostatic discharge (ESD): basics of ESD, principles of ESD control. Semiconductor Metrology: CD and overlay measurements, electrical and optical measurements. Assembly: front-end assembly and backend assembly. • Semiconductor failure analysis: implant metrology; interconnect process metrology, Ellipsometry, reflectrometry, sheet resistance measurements
Learning Outcomes	***Cognitive (Knowledge, Understanding, Application, Analysis, Evaluation, Synthesis):*** • Define key concepts relating to advance CMOS process technology. • Describe the principal stages of IC fabrication, and the tools and materials required. • Explain the physical principles involved in advanced CMOS process technology and device fabrication • Derive relevant equations describing advanced CMOS process technology, from basic laws and principles. • Solve numerical problems from information provided on the topics covered.
Recommended Text	• Robert F. Pierret (1983) Module Series on Solid State Devices , Wesley • James D. Plummer (2000) Silicon VLSI Technology , Prentice Hall
Supplementary Texts	None
Other relevant information	