

ICGEE Curriculum available for 2011/2012 Academic Year

Reconfigurable System on Chip (rSoC)

Module Title:	Reconfigurable System on Chip (rSoC) Design
Module Status:	Available, to be delivered during first semester of 2011-12 academic year

Generic Module Information:

Name of module owner/lecturer?	Dr Fearghal Morgan
Delivery mode: e.g. on-site, on-line, mixed-mode. For on-site specify contact hours per week	Workshop. Weekly web-based video link presentation to support assignment work. Available as video stream 100% assignment-based (CA) with remote FPGA laboratory access Resources: ICGEE VLE http://remoteFPGA.com (remote FPGA lab) http://www.appliedvhdl.com/course/virtual_lab/ (part 1 of course)
Duration of the module:	One semester
Assessment methods and weightings where relevant:	Continuous assessment (based on assignment submissions) No written examination Series of interlinked assignments, Project templates provided, submission checklists provided.
Pass Standard:	60%
Penalties for late submission of continuous assessment work:	10% (20%) of total marks deducted for submission 7 (14) days late. Zero mark allocation for submission 15 days late or more.
Requirements for Supplemental Examination:	N/A
Number of ECTS or institutional credits assigned to the module:	5 ECTS
Course Content or Syllabus (Optional):	<ol style="list-style-type: none"> 1. Reconfigurable (FPGA) technologies and architectures 2. Digital reconfigurable System on a Chip (rSoC) design and development process 3. Digital design and analysis techniques 4. Structured documentation methodology 5. HDL-based design capture 6. Simulation strategies 7. Logic synthesis 8. Electronic Design Automation (EDA) tools 9. Real-world considerations 10. Use of embedded processors and IP cores 11. Digital systems design and rSoC case studies
Learning Outcomes	At the end of this module the student will be able to: <ol style="list-style-type: none"> 1. Apply steps from specification to implementation of a modular, complex digital embedded reconfigurable hardware (Field Programmable Gate Array, FPGA) system. 2. Implemented hardware designs on a reconfigurable computing hardware laboratory system 3. Perform structured digital systems design 4. Review and prepare formal design and verification documentation



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	<ol style="list-style-type: none">Capture design using an industry standard HDL programming language and EDA toolsParticipate effectively within a distributed team
Pre-requisites	Basic Digital Systems Design knowledge, Programming skills
Recommended Text	Circuit Design & Simulation with VHDL, V.E. Pedroni, 2 nd Ed.
Supplementary Texts	Digital Design, Richard E. Haskell & Darrin M. Hanna